What is claimed is:

1. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion.

2. The flat panel display according to claim 1, wherein the pixel array portion and the driving circuit portion each has a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion.

3. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a driving circuit portion for driving the plurality pixels of the pixel array portion,

wherein a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film resistor in the driving circuit portion.

4. The flat panel display according to claim 3, wherein one thin film transistor of the thin film transistor in the pixel array portion and the thin film transistor in the driving circuit portion includes an offset region in its gate region.

5. The flat panel display according to claim 4, where the one thin film transistor of the thin film transistors in the pixel array portion and the driving circuit portion further includes source/drain regions, and

the offset region is a high resistance region, which is one of not doped, entirely doped and/or partially doped with impurities with the same conductivity type as the source/drain regions and has a lower concentration than the source/drain regions.

6. The flat panel display according to claim 4, wherein at the thin film transistor in the pixel array portion includes anoffset region in its gate region.

7. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein a thin film transistor in the pixel array portion has a different resistance value at least in the drain region than a thin film resistor in the driving circuit portion.

8. The flat panel display according to claim 7, wherein one of the thin film transistor of the thin film transistor in the pixel array portion and the thin film transistor in the driving circuit portion includes an offset region at least in its drain region.

9. The flat panel display according to claim 8, wherein the offset region of the one thin film transistor of the thin film transistor in the pixel array portion and the thin film transistor in the driving circuit portion is a high resistance region, which is one of not doped, entirely doped and partially doped with impurities which have the same conductivity type as the drain region and a lower concentration than the drain region.

10. The flat panel display according to claim 7, wherein the panel array portion has a plurality of thin film transistors and at least one thin film transistor of the plurality of thin film transistors in the pixel array portion includesthe offset region in its drain region.

11. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a gate driving circuit portion and a data driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion.

12. The flat panel display according to claim 11, wherein the at least one thin film transistor of the plurality of thin film transistors in the pixel array portion includes an offset region in its gate region.

13. The flat panel display according to claim 12, wherein the at least one thin film transistor of the plurality of thin film transistors in the pixel array portion further includes source/drain regions, and

the offset region is a high resistance region, which is one of not doped, entirely doped and partially doped with a low concentration of impurities of the same conductivity type as the source/drain regions.

14. The flat panel display according to claim 11, wherein the at least one thin film transistor of the plurality of thin film transistors in the pixel array portion includes an offset region at least in its drain region.

15. The flat panel display according to claim 14, wherein the offset region of the at least one thin film transistor in the pixel array portion is a high resistance region, which is one of not doped, entirely doped and partially doped with a low concentration of impurities of the same conductivity type as the drain region.

16. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein thin film transistors in the pixel array portion have different geometric structures than the driving circuit portion include gate regions.

17. The flat panel display according to claim 16, wherein at least one thin film transistor of the thin film transistors in the pixel array portion and the thin film transistors in the driving circuit portion includes a zigzag shaped gate region.

18. The flat panel display according to claim 16, wherein the gate region of at least one thin film transistor of the thin film transistors in the pixel array portion and the thin film transistors in the driving circuit portion has one of a same length and a shorter width, a same width and a longer length, and a shorter width and a longer length, than at least one other of the thin film transistors.

19. The flat panel display according to claim 17, wherein the at least one thin film transistor includes multiple gates, and further includes a high resistance offset region between the multiple gates.

20. The flat panel display according to claim 19, wherein an offset between the multiple gates in the at least one thin film transistor has a zigzag shape.

21. The flat panel display according to claim 19, wherein the offset between the multiple gates in the at least one thin film transistor has at least one of a longer length and a shorter width than the other thin film transistors.

22. The flat panel display according to claim 19, wherein at least one thin film transistor of the thin film transistors in the pixel array portion includes an offset region.

23. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein thin film transistors in the pixel array portion and the driving circuit portion include at least drain regions having different geometric structures.

24. The flat panel display according to claim 23, wherein at least one thin film transistor of the thin film transistors in the pixel array portion and the thin film transistors in the driving circuit portion includes a zigzag shaped drain region.

25. The flat panel display according to claim 23, wherein the drain region of the at least one thin film transistor of the thin film transistors in the pixel array portion and the thin film

transistors in the driving circuit portion has one of a same length and a shorter width, a same width and a longer length, and a shorter width and a longer length, than those of the other thin film transistors.

26. The flat panel display according to claim 24, wherein the drain region of the at least one thin film transistor includes a high resistance offset region.

27. The flat panel display according to claim 24, wherein a high resistance drain offset region of the at least one thin film transistor has a zigzag shape.

28. The flat panel display according to claim 24, wherein a high resistance drain offset region of the at least one thin film transistor has at least one of a longer length and a shorter width than those of the other thin film transistors.

29. The flat panel display according to claim 26, wherein at least one thin film transistor of the thin film transistors in the pixel array portion includes a high resistance region.

30. A flat panel display, comprising:

a pixel array portion having a plurality of pixels arranged thereon; and

a gate driving circuit portion and a data driving circuit portion for driving the plurality of pixels of the pixel array portion,

wherein at least one thin film transistor of thin film transistors in the pixel array portion has a different geometric structure from at least one thin film transistor of thin film transistors in the gate driving circuit portion and thin film transistors in the data driving circuit portion.

31. The flat panel display according to claim 30, wherein the at least one thin film transistor of the thin film transistors in the pixel array portion includes an offset region in one of its gate region and its drain region.

32. The flat panel display according to claim 31, wherein the offset region of the at least one thin film transistor in the pixel array portion has a zigzag shape.

33. The flat panel display according to claim 32, wherein the offset region of the at least one thin film transistor in the pixel array portion has at least one of a longer length and a shorter width than those of the other thin film transistors.